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1 General information

- Orders: Only on the email-address bestellung@hofstetter-pcb.de Note: without an present order we will not proceed the production!
 Shipping: We need to know your preferred forwarder (TNT, DHL, UPS, Forwarding Agency, Express Mail Service, etc.) as well as your required forwarding option (e.g. Express Mail Service with time options)
- Terms of payment: 10 days or as agreed
 Unauthorized payment discount will be requested

2 Information about the FinalClean process

٠	Chemistry product type:	Aurotech FinalClean, horizontal system		
•	Formats:	Min: 150 mm x 100 mm Max: 610 mm x 600 mm (other formats on request)		
•	Pcb - thickness:	Min: 0.10 mm Max: 4.50 mm (thicker formats on request)		
•	Surface finish:	ENIG (e lectroless n ickel/ i mmersion g old) or ENEPIG (e lectroless n ickel/ e lectroless p alladium/ i mmersion		

gold)

- Solderability performance ¹: No shelf life, because it is a post-processing method! After refresh APL Hofstetter recommends a prompt processing
- Ionic contamination: After the FinalClean process <0.50 µg/cm² NaCl Equivalent (measured with ENIG pcbs)

¹ Lead free solder process



3 Intake requirements before processing FinalClean

3.1 Intake requirements for pcbs

APL Hofstetter excepts only pcbs without following criteria:

- Labels
- Adhesive residues
- Condensate, oil, grease, fingerprints
- Paint flitters, solder mask residues
- Milling dust
- Twisting and warping
- Unclean multilayer cutback
- Mechanical defects (e.g. bend pcb edges, deep scratches)
- Entry opportunities of liquids (such as transition in rigid-flex-areas)
- Parts with exposed copper areas

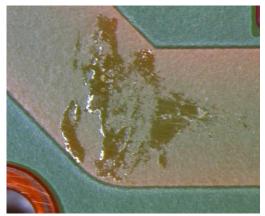


Fig. 1: condensate

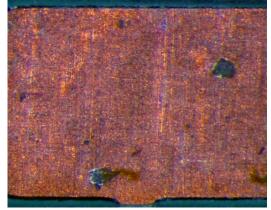


Fig. 2: solder mask residues

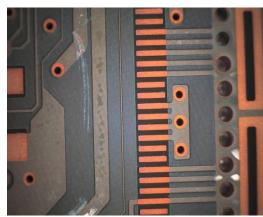


Fig. 3: mechanical solder mask defects



3.2 Intake requirements for the base material

Standard FR4 and Teflon®/ PTFE materials from global, established manufacturers are easily process able. Other materials can be made only after consultation (aluminium, ceramics etc.). Following base materials can only be processed on request:

0	FR1	0	FR2
ο	FR3	0	CEM1/CEM2

3.3 Other paints/prints

All additional lacquering or printing work prior to tinning (such as license plate lacquer, carbon lacquer, transfer printing, strippable lacquer, etc.) must be carried out in such a way that no impairments occur during the tinning process. In other words, they must be adhesive and inert. If there are justified concerns about this, processing must be rejected. If the tinning process is impaired as a result, subsequent costs (e.g. for cleaning, loss of production, etc.) will be charged.

3.4 Thermal processes

All thermal processes have to be done before the FinalClean process. All thermal processes after FinalClean (heat and cold), could lead to repeated the solderability in a negative way.

4 Terms of delivery and packaging

4.1 General information

Scribed and milled multi-panels have to be solid to minimize the risk of breaking during the FinalClean process as packaging and shipment. Paper sheets between the pcbs are not allowed because they lead to handling problems. Drying agents are neither allowed because of the risk of corrosion and/ or mechanical damages.

4.2 Packaging of incoming and outgoing pcbs²

The packaging units have to be solid for re-using and further transportation to the customers. A bigger amount of packages has to be delivered on an euro-palette. All packaging units including the content should be packed solid to protect the good against damaging. It is necessary to pack the pcbs with damping materials (damping material should be dust and lint free). The pcbs in the packaging units have to be shrunk in suitable packages (min. 10 up to max. 25 units).

5 Disclaimer of warranty

APL Hofstetter assumes no warranty for all defects which results from disregarding the general requirements and defects from the previous circuit board manufactures. FinalClean is a post-

² All used packaging materials should not influence the pcbs in a negative way.



processing method therefore APL Hofstetter will not assume warranty for following solderability of the pcbs.