HOFSTETTER
PCB PLATING

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Overview final finishes Hofstetter Group

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Process	Name	Service location	Supplier	Available on demand	Type of equipment
ENIG [4] by HOFSTETTER PCB	electroless Nickel / Gold	Herrenberg and Küssnacht	Uyemura / Umicore	✔ (Herrenberg)	vertical
ENIG TRG [4] by HOFSTETTER PCB	electroless Nickel with semi-reductive Gold	Küssnacht	Uyemura / Umicore	✔ (Herrenberg)	vertical
ENEPIG [4] by HOFSTETTER PCB	electroless Nickel / Palladium with semi-reductive Gold	Küssnacht	Uyemura / Umicore	✔ (Herrenberg)	vertical
EPIG [4] by HOFSTETTER PCB	electroless Palladium with semi-reductive Gold	Küssnacht	Uyemura / Umicore	✔ (Herrenberg)	vertical
DIG [4] by HOFSTETTER PCB	direct immersion Gold (semi-reductive)	Küssnacht	Uyemura / Umicore	✔ (Herrenberg)	vertical
immersion Sn	immersion Tin	Lörrach and Herrenberg	Atotech	✔ (Lörrach)	horizontal
immersion Ag	immersion Silver	Herrenberg and Küssnacht	MacDermid Enthone	✔ (Herrenberg)	horizontal
OSP HT	OSP High Temperatur	Herrenberg	Shikoku / Hillebrand	✔ (Herrenberg)	horizontal
elyt. Sn	electroplated Tin	Küssnacht	Schlötter	✔ (Herrenberg)	vertical
elyt. Sn / Pb	electroplated Tin / Lead	Küssnacht	DuPont	✔ (Herrenberg)	vertical
elyt. Ni / Pure Au	electroplated Nickel / Soft Gold	Küssnacht	DuPont	✔ (Herrenberg)	vertical
elyt. Ni / Au Hard	electroplated Nickel / Hard Gold	Herrenberg and Küssnacht	DuPont / Enthone	✔ (Herrenberg)	vertical
elyt. Pure Au	electroplated Direct Gold	Küssnacht	DuPont	✔ (Herrenberg)	vertical

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Process	Panel thickness min. to max. [1]	Panel size min. to max. [2]	Aspect ratio BV	Aspect ratio PTH	Shelf Life [5]
ENIG [4] by HOFSTETTER PCB	0.012 mm to 16 mm	100 × 100 mm to 610 × 610 mm	1 : 1	1 : 16	12 Months
ENIG TRG [4] by HOFSTETTER PCB	0.012 mm to 16 mm	100 × 100 mm to 610 × 610 mm	1 : 1	1 : 16	12 Months
ENEPIG [4] by HOFSTETTER PCB	0.012 mm to 16 mm	100 × 100 mm to 610 × 610 mm	1 : 1	1 : 16	12 Months
EPIG [4] by HOFSTETTER PCB	0.012 mm to 16 mm	100 × 100 mm to 610 × 610 mm	1 : 1	1 : 16	12 Months
DIG [4] by HOFSTETTER PCB	0.012 mm to 16 mm	100 × 100 mm to 610 × 610 mm	1 : 1	1 : 16	3 – 6 Months [12]
immersion Sn	0.012 mm to 5 mm	100 × 60 mm to 610 × 2000 mm [3]	1 : 1	1 : 16	6 Months
immersion Ag	0.012 mm to 6 mm	100 × 60 mm to 610 × 2000 mm [3]	1 : 1	1 : 16	12 Months
OSP HT	0.012 mm to 5 mm	100 × 60 mm to 610 × 2000 mm [3]	1 : 1	1 : 16	6 Months
elyt. Sn	0.012 mm to 20 mm	100 × 60 mm to 610 × 1800 mm	1 : 1	1 : 16	12 Months
elyt. Sn / Pb	0.012 mm to 20 mm	100 × 60 mm to 610 × 1800 mm	1 : 1	1 : 16	12 Months
elyt. Ni/Pure Au	0.012 mm to 20 mm	100 × 60 mm to 610 × 1100 mm	1 : 1	1 : 12	12 Months
elyt. Ni/Au Hard	0.012 mm to 20 mm	100 × 60 mm to 610 × 1100 mm	1 : 1	1 : 12	12 Months
elyt. Pure Au	0.012 mm to 20 mm	100 × 60 mm to 610 × 1100 mm	1 : 1	1 : 12	12 Months

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Process	Layer 1	Thickness 1	Layer 2	Thickness 2	Layer 3	Thickness 3
ENIG [4] by HOFSTETTER PCB	Nickel	3 – 7 µm [6]	Gold	0.05 – 0.1 µm	n.a.	
ENIG TRG [4] by HOFSTETTER PCB	Nickel	3 – 7 µm [6]	Gold	0.05 – 0.1 µm [7]	n.a.	
ENEPIG [4] by HOFSTETTER PCB	Nickel	3 – 7 µm [6]	Palladium	0.08 – 0.3 µm [8]	Gold	0.03 – 0.08 µm [7]
EPIG [4] by HOFSTETTER PCB	Palladium	0.1 – 0.2 µm [9]	Gold	0.1 – 0.2 µm [7]	n.a.	
DIG [4] by HOFSTETTER PCB	Gold	0.2 – 0.3 µm [10]	n.a.		n.a.	
immersion Sn	Tin	0.6 – 1.2 µm [11]	n.a.		n.a.	
immersion Ag	Silver	0.15 – 0.4 µm	n.a.		n.a.	
OSP HT	OSP	0.15 – 0.3 µm	n.a.		n.a.	
elyt. Sn	Tin	5 – 15 µm	n.a.		n.a.	
elyt. Sn / Pb	Tin / Lead	5 – 15 µm	n.a.		n.a.	
elyt. Ni/Pure Au	Nickel	3 – 10 µm	Gold	0.1 – 10 µm	n.a.	
elyt. Ni/Au Hard	Nickel	3 – 8 µm	Gold	0.2 – 10 µm	n.a.	
elyt. Pure Au	Gold	> 3 µm	n.a.		n.a.	

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Classification

- (++) excellent
- (+) good
- (0) with restrictions
- (-) poor
- (--) not recommended

Suitable for:

Process	ead-free solder	Leaded solder	Gold wire bonding	Aluminum wire bonding	Press-fit	Connectors	High frequency application	Fineline (< 30 µm)	Button connectors	Corrosion resistance	Reworkability	Storage + Packaging
ENIG [4] by HOFSTETTER PCB	(+)	(+)	(-)	(+)	0	0	(--)	(-)	0	0	(--)	(+)
ENIG TRG [4] by HOFSTETTER PCB	(++)	(++)	0	(--)	0	0	(--)	(-)	0	0	(--)	(+)
ENEPIG [4] by HOFSTETTER PCB	(++)	(-)	(++)	(++)	0	(+)	(--)	(-)	(+)	(+)	(--)	(++)
EPIG [4] by HOFSTETTER PCB	(++)	(+)	(+)	(+)	0	(-)	(+)	0	0	0	(--)	0
DIG [4] by HOFSTETTER PCB	(++)	(++)	(+)	(-)	0	(--)	(++)	(++)	(--)	(--)	(+)	(-)
immersion Sn	(+)	(+)	(--)	(--)	(++)	(--)	(+)	0	(--)	0	(++)	(-)
immersion Ag	(+) [14]	(+) [14]	(--)	(--)	0	(--)	(++)	0	(--)	(-)	0	(-)
OSP HT	(+) [14]	(+) [14]	(--)	(--)	(--)	(--)	(+)	(+)	(--)	(--)	(++)	(-)
elyt. Sn	(++)	(++)	(--)	(--)	(++)	(-)	(0)	(-)	(-)	(+)	(+)	(+)
elyt. Sn / Pb	(++)	(++)	(--)	(--)	(++)	(-)	(0)	(-)	(-)	(+)	(+)	(+)
elyt. Ni/Pure Au	(+)	(+)	(++)	(+)	0	(+)	(--)	(-)	(+)	(++)	(-)	(++)
elyt. Ni/Au Hard	(--)	(--)	(--)	(--)	0	(++)	(--)	(-)	(++)	(++)	(-)	(++)
elyt. Pure Au	(+)	(+)	(+)	0	0	0	(+)	0	(+)	(+)	(+)	0

An extensive range of unleaded sur-faces finishes for complex technical requirements.

Legend

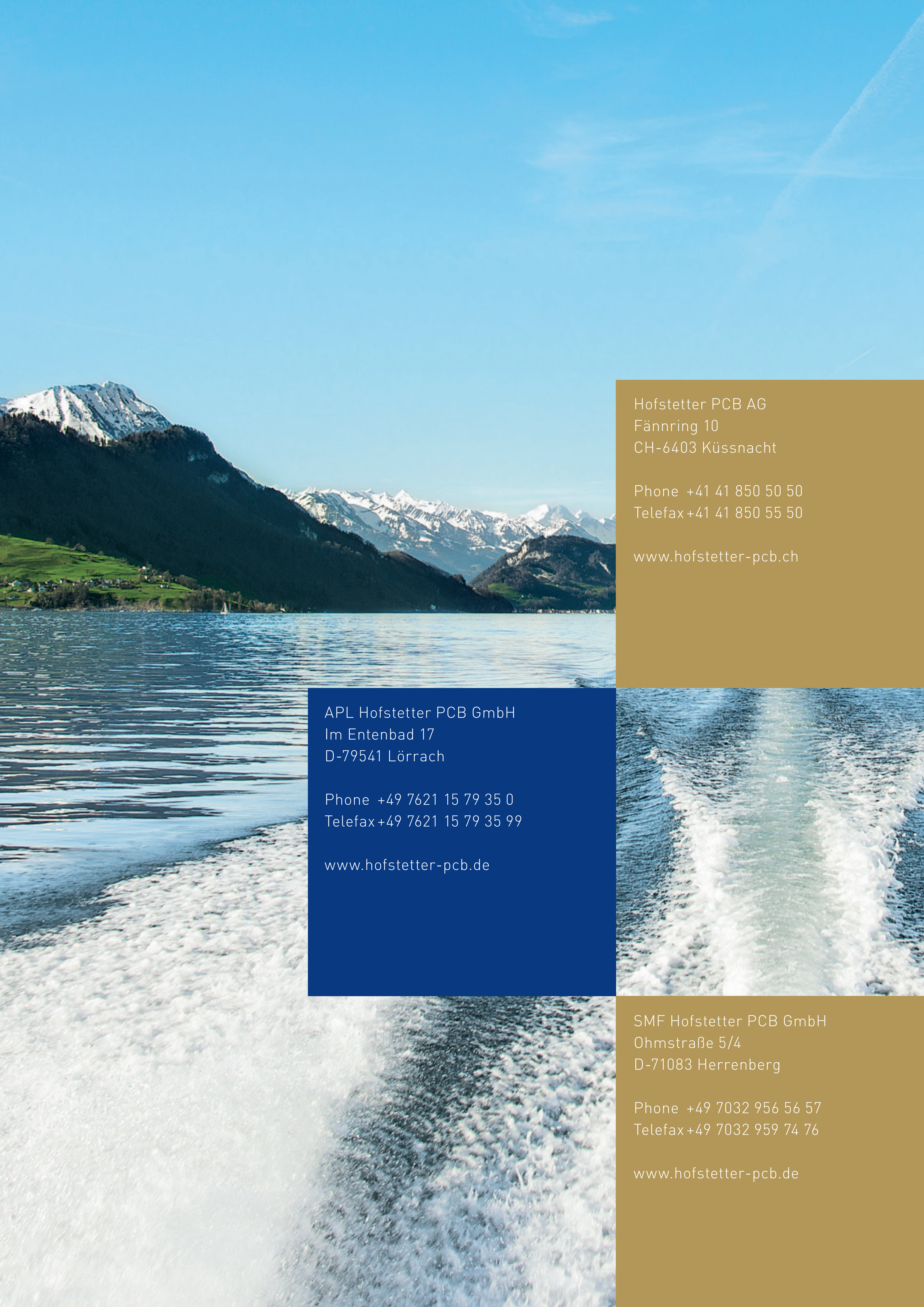
1) Other panel thicknesses on request.
2) Other panel thicknesses on request.
3) Reel to Reel possible.
4) Additional pre-treatment may be necessary after consultation, depending on base material i.e. (tempering in Herrenberg and Küssnacht possible) (plasma, jet pumice, permanganate, tin stripping in Küssnacht possible).
5) Other layer thicknesses can lead to changes. Important: Correct packaging and storage conditions (please note specifications).
6) 1.5 µm – 10 µm possible (Upper range min. 2 µm).
7) Layer thicknesses up to max. 0.2 – 0.3 µm possible with semi-reductive gold bath (range over 0.1 µm layer thickness, always minimum 0.1 µm deviation).
8) Layer thicknesses greater than 0.3 µm possible, but no advantage.
9) Higher layer thicknesses possible, above 0.4 µm is not recommended.
10) Maximum layer thickness 0.2 – 0.3 µm, lower layer thicknesses possible for pure soldering applications and after testing, minimum layer thickness 0.1 – 0.2 µm. Depending on the pattern and material, the min / max value must be adjusted, because the variations are bigger. This assessment can only be made after the plating.
11) Maximum layer thickness 1.2 µm (1.2 µm only possible with two runs)
12) Depending on the application.
13) Different materials behave differently. It is not always possible to make a general statement. We recommend asking and or even better, having material tested with a relevant pattern design.
14) From 2× reflow steps, various influences can have a negative effect (e.g. a long waiting time between individual reflow steps).

General delivery condition:

A) Soldermask as well as electrolytic gold resists must be completely polymerized (resists are not allowed in electroless final finishes). Use of peelable soldermask is allowed.
B) Through holes MUST be completely open or completely closed. Otherwise no guarantee can be given for a successful plating, especially in electroless processes.
C) Copper must be free of any contamination, residues of soldermask or resist prevent plating at the affected areas and/or cause problems with the plating (pretreatment is possible after consultation).
D) Maximum aspect ratio 1:1 of blind vias in the plated condition.
E) Panels from stock have to be desoxidized and dry before sending to us.
F) LDI and DI masks have to be additionally UV bump cured.
G) In electrolytic processes, all surfaces to be plated must be connected with sufficient electric conductor cross-section (contact for galvanic Sn and SnPb over long edge, for galvanic Ni / Au over short edge possible).

Information on delivery note and on request for quotation

A) Ordered final finish with process name e.g. ENEPIG by Hofstetter PCB or galv. Ni / Bondgold etc.
B) Layer thickness of each layer with range e.g. nickel 3 – 7 µm / palladium 0.08 – 0.20 µm / gold 0.03 – 0.08 µm (mean value is the target value) or indication of the minimum layer thickness (mostly galv. gold) nickel min. 4 µm / gold min. 1.0 µm.
C) Indication of the complete active surface area incl. panel frame and surface of the holes, especially for processes where precious metals such as palladium and gold are required.
D) Length, width and material thickness of the panel
E) Blind holes yes / no, if yes which aspect ratio.
F) Requested delivery date at leaving Hofstetter site.
G) Specification of outer layer material (especially for final finishes such as ENIG / ENIG TRG / ENEPIG / EPIG / ISIG / DIG).
H) Specification of solder mask type requested.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